## **AMENDMENTS TO THE SPECIFICATION**

Please replace the title beginning on page 1, line 3, with the following amended title:

Technical Field of the Invention

Please replace the paragraph beginning on page 1, line 5 with the following amended paragraph:

The present invention relates to a semiconductor device; and, more particularly, to a A semiconductor device is disclosed which is capable of preventing a pattern collapse in an edge area in on a semiconductor wafer.

Please replace the paragraph beginning on page 2, line 1 with the following amended paragraph:

Due to a current trend of high integration of the semiconductor device devices, bar-type patterns are formed in the cell edge area through the same condition of forming the line patterns in a cell center area in order to improve line width uniformity.

Please replace the paragraph beginning on page 2, line 6 with the following amended paragraph:

It is an object of the present invention to provide a A semiconductor device is therefore needed that is capable of preventing a pattern collapse phenomenon in an area, where a pattern becomes fragile, for instance, in a cell edge area.

Please replace the title beginning on page 2, line 11 with the following amended title:

Summary of the Invention Disclosure

Please replace the paragraph beginning on page 2, line 13 with the following amended paragraph:

In accordance with an aspect of the present invention, the inventive A disclosed semiconductor device having comprises a lower pattern density in an edge area than in a central area of a wafer; includes a plurality of bar-type patterns allocated at a

predetermined distance in the central area of the wafer; a plurality of dummy patterns formed in the edge area; and a plurality of a connection pattern for coupling at least two of the bartype patterns to each other, wherein the connection patterns of the plurality of dummy patterns is allocated in are disposed offset from one another in a zigzag fashion.

Please replace the paragraph beginning on page 2, line 26 with the following amended paragraph:

The above and other objects and features of the present invention disclosed semiconductor devices will become apparent from the following description of preferred embodiments taken in conjunction with the accompanying drawings, in which wherein:

Please replace the paragraph beginning on page 3, line 3 with the following amended paragraph:

Fig. 1 is a plane plan view illustrating bar-type patterns formed in cell center and edge areas of a conventional semiconductor device;

Please replace the paragraph beginning on page 3, line 9 with the following amended paragraph:

Fig. 3 is a diagram of a scanning electron microscope SEM micrograph showing a plane plan view of the pattern collapse of a dummy pattern in the cell edge area of the conventional semiconductor device;

Please replace the paragraph beginning on page 3, line 13 with the following amended paragraph:

Figs. 4A and 4B are diagrams of SEM micrographs showing the pattern collapse of the bar pattern in the cell edge area of the conventional semiconductor device;

Please replace the paragraph beginning on page 3, line 15 with the following amended paragraph:

Fig. 5 is a plane plan view of a <u>disclosed</u> semiconductor device completed with a predetermined process for forming a bar pattern in accordance with a preferred embodiment of the present invention; and

Please replace the paragraph beginning on page 3, line 19 with the following amended paragraph:

Fig. 6 is a diagram of a SEM micrograph showing a plane plan view of the semiconductor device described in Fig. 5.

Please replace the title beginning on page 3, line 22 with the following amended title:

Detailed Description of the Invention Presently Preferred Embodiments

Please replace the paragraph beginning on page 3, line 24 with the following amended paragraph:

Referring to FIGS. 1-4B, a conventional semiconductor device is generally shown. Fig. 1 is a plane plan view illustrating bar-type patterns formed in cell center and edge areas of a conventional semiconductor device. Fig. 2 is a explanatory diagram for describing a pattern collapse in the cell edge area of the conventional semiconductor device, and Fig. 3 is a diagram of a scanning electron microscope SEM micrograph showing a plane view of the pattern collapse of a dummy pattern in the cell edge area in where the bar-type patterns are formed.

Please replace the paragraph beginning on page 4, line 7 with the following amended paragraph:

As shown in Fig. 1, a plurality of the bar-type patterns 10A are formed with a predetermined distance  $\frac{d}{D}$  in the cell center and edge areas. A plurality of the dummy patterns 10B are formed in the cell edge area.

Please replace the paragraph beginning on page 5, line 6 with the following amended paragraph:

Referring to FIGS. 5 and 8 6, a semiconductor device capable of preventing pattern collapse in accordance with the present invention is generally shown. The present invention disclosed device is designed under the basic principle that a pattern collapse phenomenon can be effectively overcome in case that a contact surface area between a pattern and a lower layer, e.g., an insulation layer, is large. For minimizing a proximity effect

that occurs in a cell edge area by limitation of photo-lithography, at least several to dozens of dummy patterns are formed in the cell edge area and these dummy patterns have a similar site to bar-patterns formed in the whole cell area. Also, there are conditions to form effectively isolated bar-patterns minimized with the proximity effect. First, isolated bar patterns formed in the cell edge area are the dummy patterns. Furthermore, dummy patterns are regularly connected to each other in order to effectively present the pattern collapse among the dummy patterns and increase the contact surface area of the bar-pattern with the lower layer.

Please replace the paragraph beginning on page 5, line 24 with the following amended paragraph:

Hereinafter, a <u>disclosed</u> semiconductor device according to the present invention will be described in detail referring to the accompanying drawings.

Please replace the paragraph beginning on page 5, line 27 with the following amended paragraph:

Fig. 5 is a plane plan view of a semiconductor device completed with a predetermined process for forming a bar pattern in accordance with a preferred embodiment of the present invention.

Please replace the paragraph beginning on page 6, line 4 with the following amended paragraph:

As shown, in the <u>inventive disclosed</u> semiconductor device, there is a semiconductor memory cell 50 of which size gets smaller because the bar-pattern has less topology in a cell edge area B-B' than in a cell center area A-A'. The semiconductor memory device includes a plurality of the <u>active</u> bar-type patterns 51 formed in the cell center area A-A' except for the cell edge area B-B', and a connection pattern 52C connecting at least two <u>dummy</u> bar-type patterns 52A and 52B to each other for protecting the bar patterns 52A and 52B from being collapsed. Herein, the <u>dummy</u> bar-type patterns 52A and 52B are formed in the cell edge area B-B' of the semiconductor memory cell 50. Also, the bar-type patterns 52A and 52B and the connection pattern 52c are a dummy pattern.

Please replace the paragraph beginning on page 7, line 9 with the following amended paragraph:

As shown in Fig. 5, the <u>parallel dummy</u> bar-type patterns 52A and 52B have less adhesive force to the layer beneath than those in the cell center area A-A'. The dummy patterns produced by connecting at least the two bar-type patterns 52A and 52B to each other throughout through the perpendicular connection pattern 52C for increasing the contact surface area with the lower layer enhance the adhesive force. The connection pattern patterns 52C is are not a straight pattern but are offset or staggered with respect to each other to form a zigzag pattern. Namely, a plurality of the connection pattern patterns 52C is are allocated in zigzags a zigzag pattern or offset from one another for connecting the two bar-type patterns in the cell edge area B-B'. In other words, adjacent connecting patterns 52C are staggered or offset and do not form a straight line as they extend along the wafer 50 as shown in FIG. 5.

Please replace the paragraph beginning on page 8, line 5 with the following amended paragraph:

In accordance with the preferred embodiment of the present invention, the bartype dummy patterns are formed by connecting at least two bar-type patterns through the use of the connection pattern in the cell edge area to thereby increase the contact area of the bartype dummy patterns with the lower layer. This increased contact area provides a further effect of preventing the pattern collapse in the cell edge area.

Please replace the paragraph beginning on page 8, line 13 with the following amended paragraph:

For example, the preferred embodiment of the present invention provides an example of a cell using a device isolation layer and a landing plug contact as the bar-type pattern. However, the bar-type pattern can be also applied not only to a conductibility pattern such as a bit line, a word line, a metal wire, and so on but also to other various types of patterns.

Please replace the paragraph beginning on page 8, line 20 with the following amended paragraph:

While the present invention has been described with respect to the particular embodiments have been shown and disclosed, it will be apparent to those skilled in the art that various changes and modification may be made without departing from the spirit and scope of the invention as defined in this disclosure and the following claims: